

74LVC2G241

Dual buffer/line driver; 3-state

Rev. 08 — 12 March 2008

Product data sheet

1. General description

The 74LVC2G241 is a dual non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE:

- A HIGH level at pin $1\overline{OE}$ causes output 1Y to assume a high-impedance OFF-state.
- A LOW level at pin 2OE causes output 2Y to assume a high-impedance OFF-state.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of the 74LVC2G241 as a translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

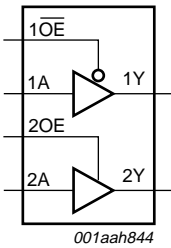
Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G241DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G241DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G241GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G241GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

4. Marking

Table 2. Marking codes

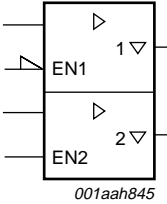
Type number	Marking code
74LVC2G241DP	V241
74LVC2G241DC	V41
74LVC2G241GT	V41
74LVC2G241GM	V41

5. Functional diagram



001aah844

Fig 1. Logic symbol



001aah845

Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

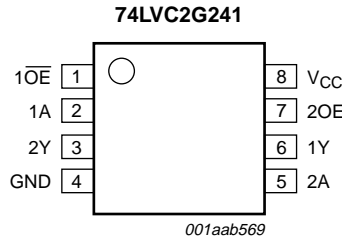


Fig 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

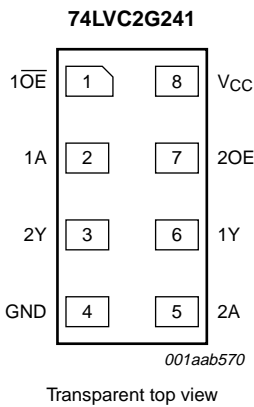


Fig 4. Pin configuration SOT833-1 (XSON8)

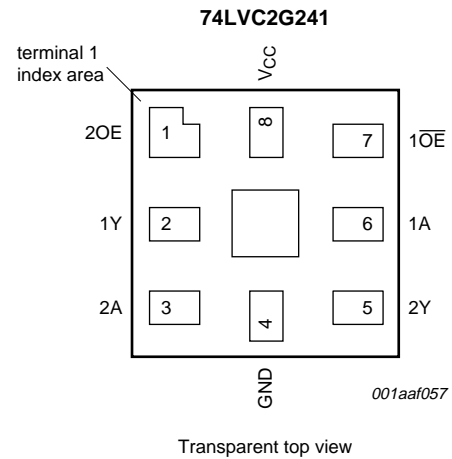


Fig 5. Pin configuration SOT902-1 (XQFN8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1 and SOT833-1	SOT902-1	
1OE	1	7	output enable input 1 (active LOW)
1A	2	6	data input 1
2Y	3	5	data output 2
GND	4	4	ground (0 V)
2A	5	3	data input 2
1Y	6	2	data output 1
2OE	7	1	output enable input 2 (active HIGH)
VCC	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input				Output	
1OE	1A	2OE	2A	1Y	2Y
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	enable mode	[1] -0.5	$V_{CC} + 0.5$	V
		disable mode	[1] -0.5	+6.5	V
		Power-down mode	[1][2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly at 2.5 mW/K.
 For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly at 8.0 mW/K.
 For XSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly at 2.4 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	$V_{CC} = 1.65\text{ V to }5.5\text{ V; enable mode}$	0	V_{CC}	V
		$V_{CC} = 1.65\text{ V to }5.5\text{ V; disable mode}$	0	5.5	V
		$V_{CC} = 0\text{ V; Power-down mode}$	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\ \mu\text{A; }V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA; }V_{CC} = 1.65\text{ V}$	-	-	0.45	V
		$I_O = 8\text{ mA; }V_{CC} = 2.3\text{ V}$	-	-	0.3	V
		$I_O = 12\text{ mA; }V_{CC} = 2.7\text{ V}$	-	-	0.4	V
		$I_O = 24\text{ mA; }V_{CC} = 3.0\text{ V}$	-	-	0.55	V
		$I_O = 32\text{ mA; }V_{CC} = 4.5\text{ V}$	-	-	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\ \mu\text{A; }V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA; }V_{CC} = 1.65\text{ V}$	1.2	-	-	V
		$I_O = -8\text{ mA; }V_{CC} = 2.3\text{ V}$	1.9	-	-	V
		$I_O = -12\text{ mA; }V_{CC} = 2.7\text{ V}$	2.2	-	-	V
		$I_O = -24\text{ mA; }V_{CC} = 3.0\text{ V}$	2.3	-	-	V
		$I_O = -32\text{ mA; }V_{CC} = 4.5\text{ V}$	3.8	-	-	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND; }V_{CC} = 0\text{ V to }5.5\text{ V}$	-	± 0.1	± 5	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	-	±0.1	±10	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±10	µA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	0.1	10	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	5	500	µA
C _I	input capacitance		-	2	-	pF
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±20	µA
		V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	-	-	±20	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	-	±20	µA
I _{CC}	supply current	V _I = 5.5 V or GND; I _O = 0 A; V _{CC} = 1.65 V to 5.5 V	-	-	40	µA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.3 V to 5.5 V	-	-	5	mA

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.5	8.8	1.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.8	4.9	0.5	6.3	ns
		V _{CC} = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.6	4.3	0.5	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.1	3.7	0.5	4.6	ns
t _{en}	enable time	1OE to 1Y; see Figure 7 ^[3]						
		V _{CC} = 1.65 V to 1.95 V	1.5	5.2	9.9	1.5	12.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.1	5.6	1.0	7.0	ns
		V _{CC} = 2.7 V	1.5	3.2	5.5	1.5	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.7	4.7	0.5	5.9	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.8	0.5	4.8	ns
		2OE to 2Y; see Figure 8 ^[3]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.3	8.8	1.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.7	4.7	1.0	5.9	ns
		V _{CC} = 2.7 V	1.0	2.7	4.6	1.0	5.8	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.1	1.0	5.1	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.9	3.3	0.5	4.1	ns
t _{dis}	disable time	1OE to 1Y; see Figure 7 ^[4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.2	11.6	1.0	14.1	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	5.8	0.5	7.6	ns
		V _{CC} = 2.7 V	1.0	2.8	4.6	1.0	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.6	4.4	1.0	5.7	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.4	0.5	4.6	ns
		2OE to 2Y; see Figure 8 ^[4]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.6	12.5	1.0	15.2	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.0	5.2	0.5	6.9	ns
		V _{CC} = 2.7 V	1.5	3.2	4.9	1.5	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.8	4.2	1.0	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	2.0	3.3	0.5	4.4	ns

Table 8. Dynamic characteristics ...continued
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ^[5]						
		output enabled	-	20	-	-	-	pF
		output disabled	-	5	-	-	-	pF

- [1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] t_{en} is the same as t_{PZH} and t_{PZL}.
- [4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms

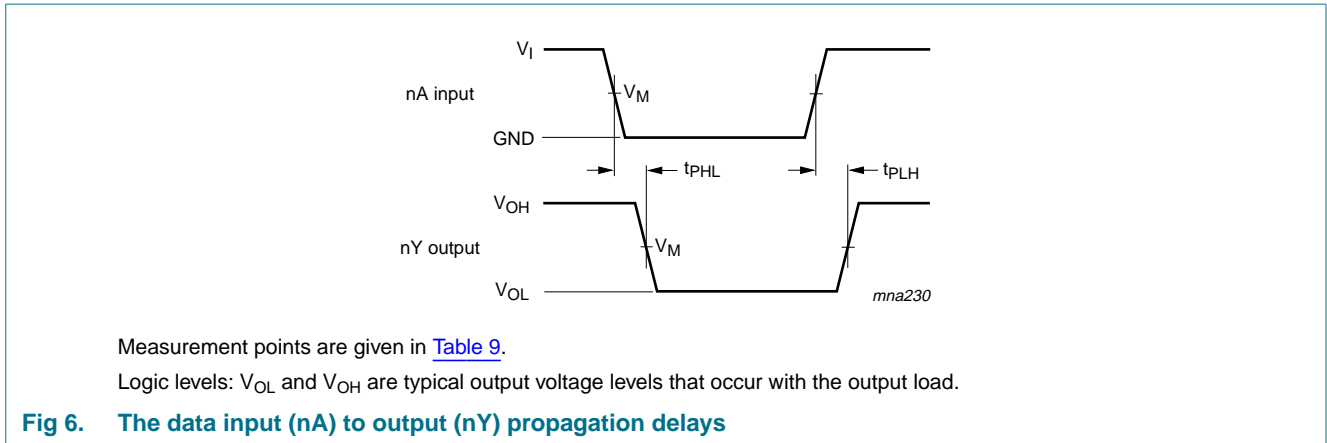
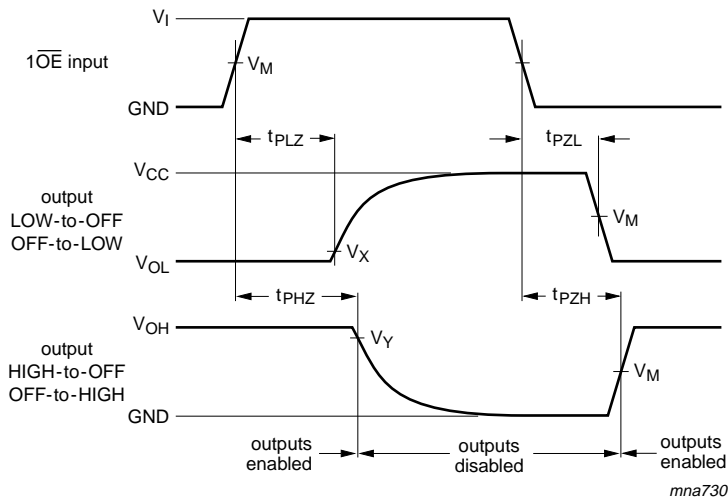


Table 9. Measurement points

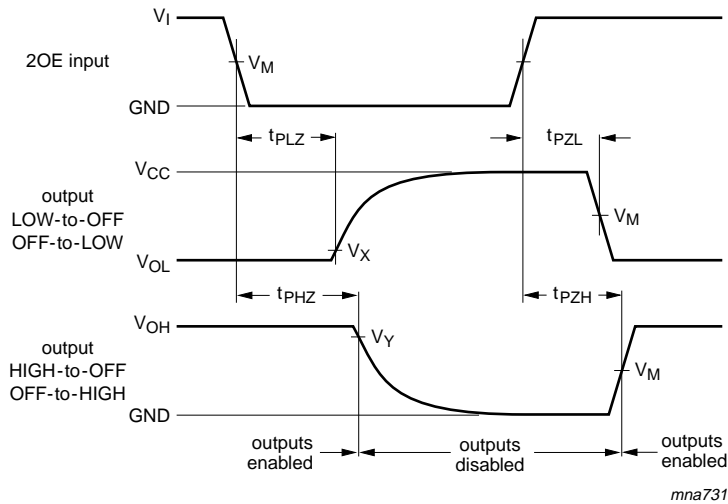
Supply voltage	Input	Output		
V _{CC}	V _M	V _M	V _X	V _Y
1.65 V to 1.95 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.3 V to 2.7 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
4.5 V to 5.5 V	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

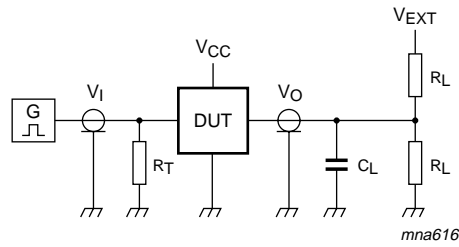
Fig 7. Enable and disable times for input 1OE



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Enable and disable times for input 2OE



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input	Load		V_{EXT}		
	V_I	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

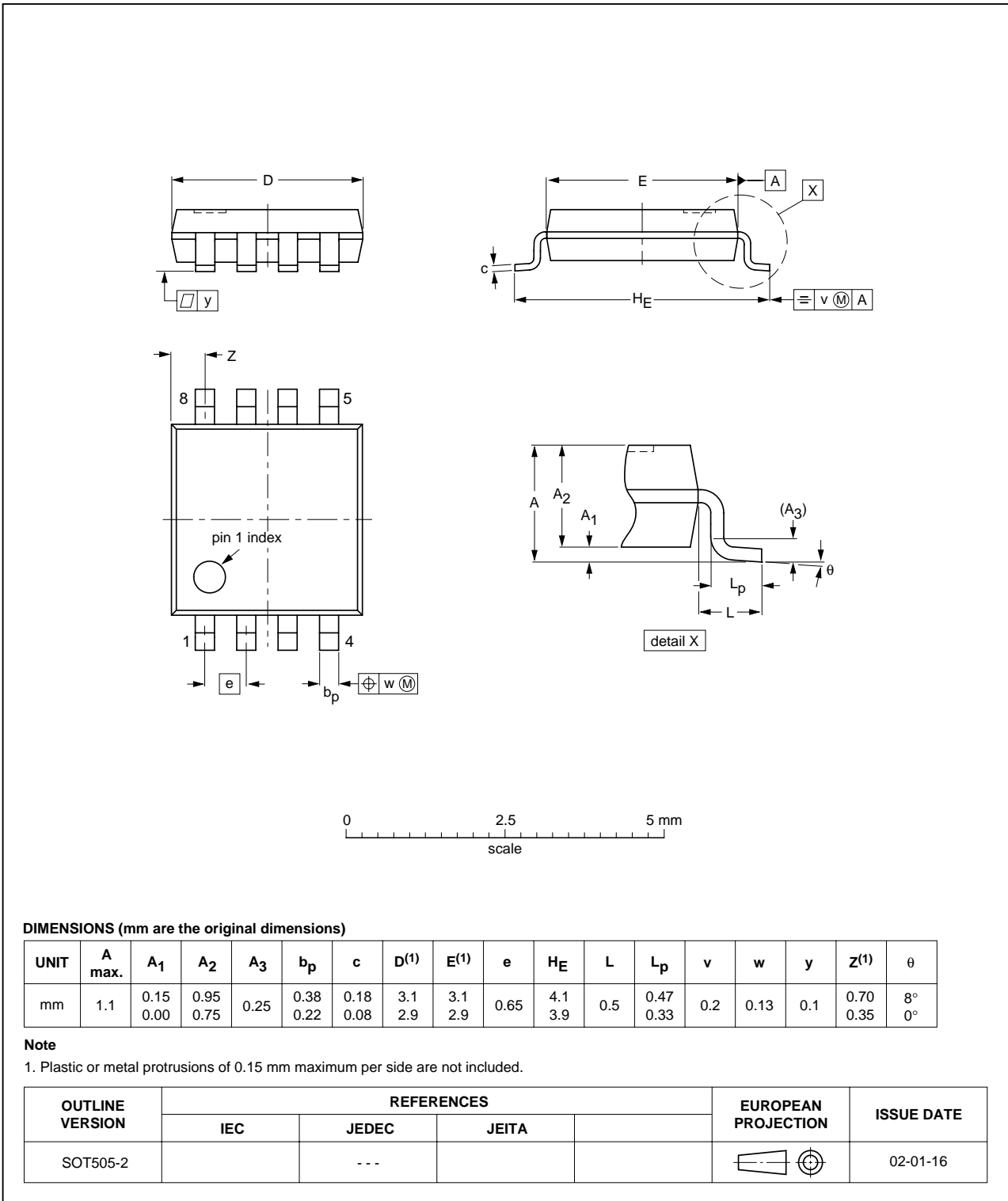


Fig 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

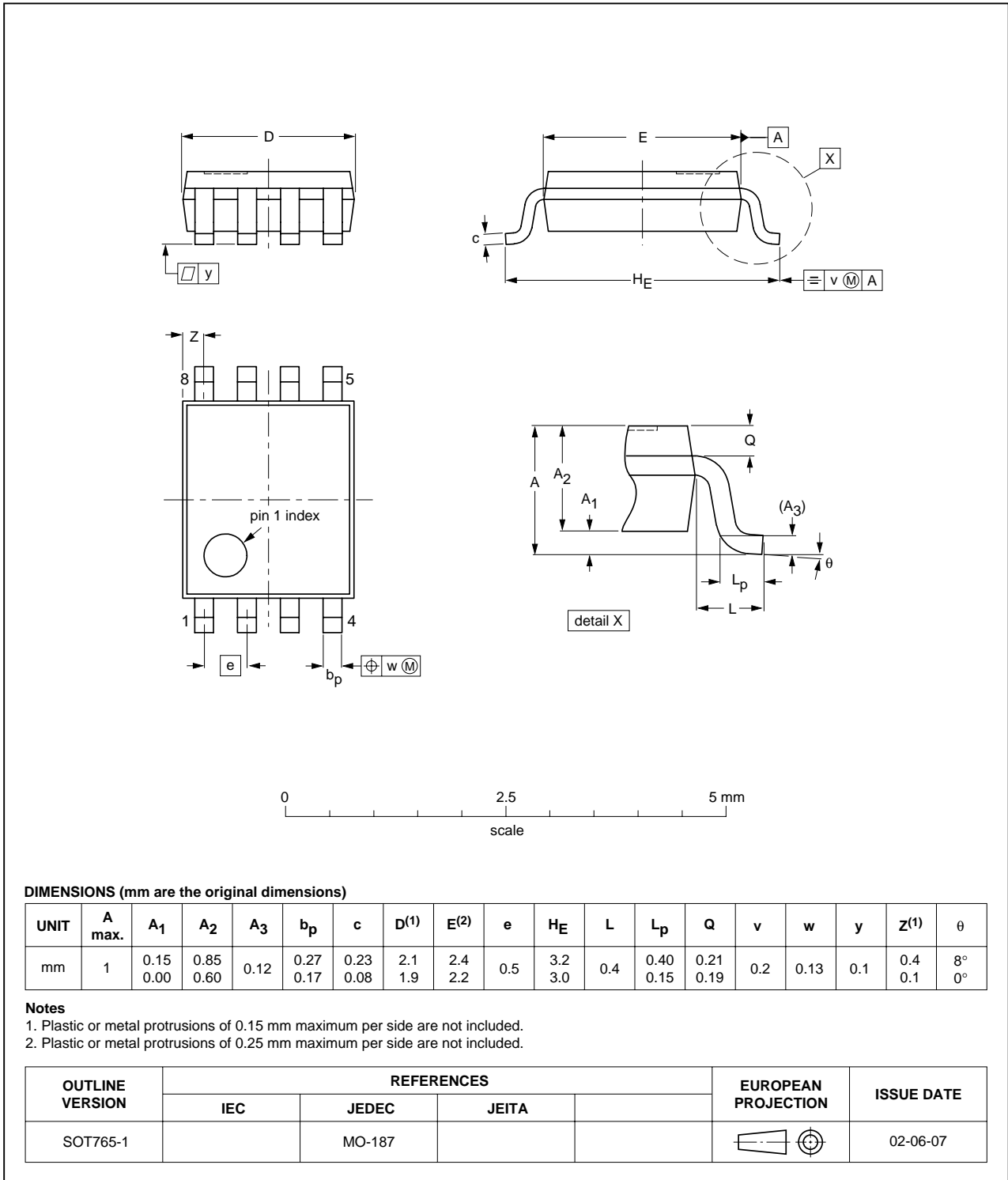


Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

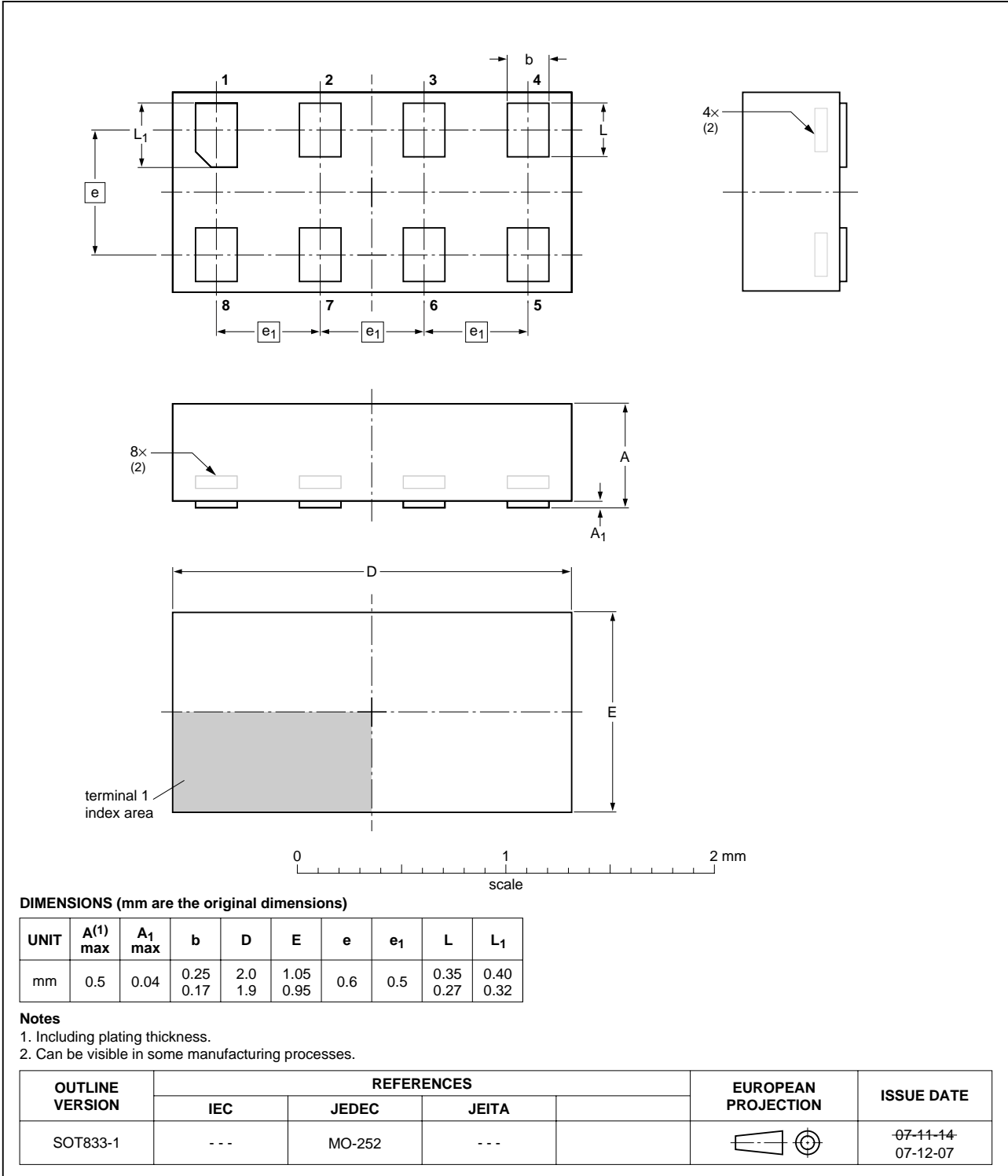


Fig 12. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads;
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

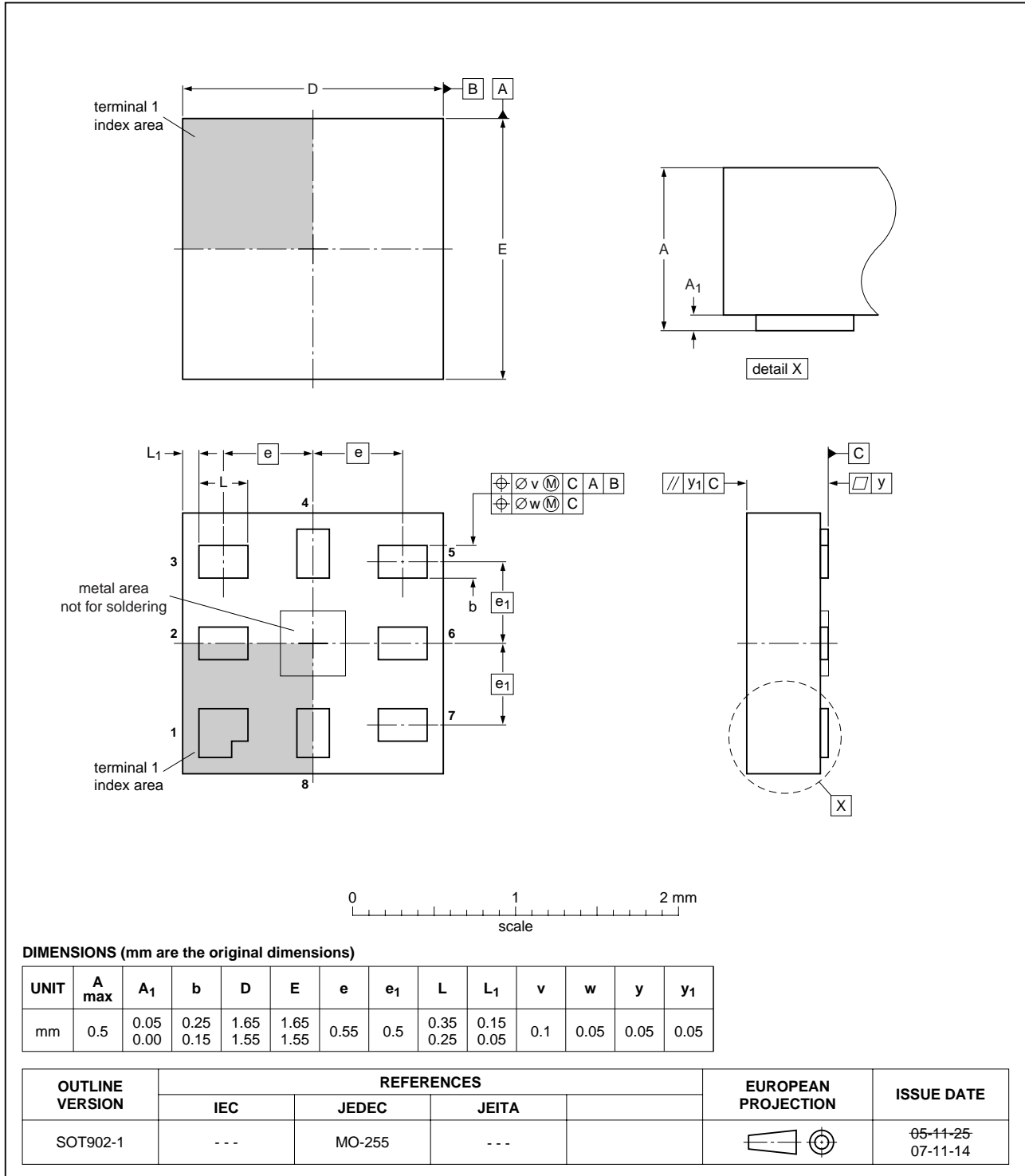


Fig 13. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G241_8	20080312	Product data sheet	-	74LVC2G241_7
Modifications:	<ul style="list-style-type: none"> • Figure 1 and Figure 2: pin numbers removed from logic symbols • Figure 13: package outline drawing updated to latest version 			
74LVC2G241_7	20071005	Product data sheet	-	74LVC2G241_6
74LVC2G241_6	20060922	Product data sheet	-	74LVC2G241_5
74LVC2G241_5	20050202	Product specification	-	74LVC2G241_4
74LVC2G241_4	20040922	Product specification	-	74LVC2G241_3
74LVC2G241_3	20030311	Product specification	-	74LVC2G241_2
74LVC2G241_2	20030129	Product specification	-	74LVC2G241_1
74LVC2G241_1	20021030	Product specification	-	-

16. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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